REMARKS

The application has been reviewed in light of the Office Action mailed April 19, 2004. At the time of the Office Action, Claims 1-28 were pending in this application. Claims 1-28 were rejected.

Rejections under 35 U.S.C. § 112, First Paragraph

Claims 1-28 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The rejection asserts that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses the rejections and submits that the specification and claims as originally filed would enable one skilled in the art of digital circuits to practice the invention without undue experimentation.

Applicant respectfully submits the following example of how the invention is practiced for one having ordinary skill in the relevant art. A maximally positive signed fractional number is defined as the largest positive number that can be represented in the number of bits available in a fixed point signed fractional operand. In the case of a 16-bit operand where the fractional point is located immediately to the right of the most significant bit, that number is:

Hex: Ox7FFF
Binary: %0111 1111 1111 1111
Decimal: +0.999969482

A maximally negative signed fractional number is defined as the largest negative number that can be represented in the number of bits available in a fixed point signed fractional

operand. In the case of a 16-bit operand where the fractional point is located immediately to the right of the most significant bit, that number is:

Hex: 0x8000
Binary: %1000 0000 0000 0000
Decimal: -1.0

By way of example to demonstrate the problem, consider the multiplication of -1 x -1. In hex, the problem can be represented as:

0x8000 X 0x8000

The result should be Decimal: +1.0. However, multiplying 0x8000 x 0x8000 using a 16-bit signed multiplier will produce the 32-bit result of 0x40000000.

0x8000 x 0x8000 = 0x40000000

Because the operands are fixed point fractional values, the fractional point of this result is now between bit 29 and bit 30 of this result (where the LS-bit of the result is regarded as bit 0). The result must therefore be shifted left by 1 to "align" the fractional points of the operand and the result, such that the result fractional point is now located immediately to the right of the most significant bit. The LS-bit of the result is now vacant and is filled with a 0.

Note that this operation is executed for all fractional multiply operations and allows the most significant (MS) 16-bit word of a 32-bit fractional result to be saved as a 16-bit fractional value without any adjustment.

0x8000 x 0x8000 = 0x40000000
0x40000000 <<1 = 0x80000000 = -1

From the example above, it can be seen that the result of -1 X -1 using a 16-bit fractional (*i.e.*, with the left shift by 1 in place) signed multiplier is -1 (not +1 as it should be). So, there's a need

for some means to correct this value (the reason this happens is because the multiplier has overflowed the (MS) sign bit).

One known method is to use a 17-bit multiplier. The operands are sign extended to 17-bits and the result will be a 34-bit value. The math then becomes:

0x08000 X 0x08000 = 0x40000000
0x40000000 <<1 = 0x80000000 = +1

The fractional point of the operands is located between bit 14 and bit 15 of the operand (as before). Multiplying two 17-bit numbers produces a 34-bit result, but the fractional point will still be located between bit 29 and bit 30 of the result (as before). The shift operation moves the fractional point to between bits 30 and 31 (as before) but there are now valid integer bits in the result. The value 0x80000000 can therefore be correctly interpreted as +1.

An alternative solution is use a fractional multiplier and detect that the operands being multiplied are 0x8000 and 0x8000. The result would then be forced to the positive number as close to +1 as possible. In the case of a 32-bit result, that would be 0x7FFFFFFF (almost +1). In the case of a 33-bit (or greater) result, that would be 0x080000000 (exactly +1). But this requires a fair amount of extra hardware around the multiplier.

According to a specific embodiment of the present invention, a 16-bit multiplier examines the result prior to the shift. It can be shown that the only case where the (pre-shift) result is 0x40000000 is when the input operands are both 0x8000. By detecting when bit 31 and bit 30 of the result is equal to binary %01 (*e.g.*, by a simple 2 input gate), hardware can take appropriate action to correct the (shifted) result. One option is to simply complement the result:

0x8000 x 0x8000 = 0x40000000
0x40000000 << 1 = 0x80000000

Pre-shift result bits 31:30 = %01, so complement final result:

! 0x80000000 = 0x7FFFFFFF

The result is very close to +1 (close enough for all practical purposes, though it does introduce some error).

An alternative approach is to create a 33-bit result where the MS-bit is a sign extension of the result except when bit 31 and bit 30 of the pre-shifted result is equal to binary %01 (*i.e.*, when the operands are both 0x8000), in which case it is cleared:

0x8000 x 0x8000 = 0x40000000
0x40000000 << 1 = 0x80000000
Sign extend result into bit 33, so result = 0x180000000
Pre-shift result bits 31:30 = %01, so clear bit 33:
Final result = 0x080000000 = +1

Therefore, determining that bits 31:30 = binary %01 after multiplying two 16 bit values to produce a 32 bit result will represent that the two 16 bit values were maximally negative fractional numbers, as clearly disclosed in the limitations of the claims, and throughout the specification and drawing figures as originally filed.

Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 5 and 19 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have been amended, as helpfully suggested by the examiner, to more clearly point out and distinctly claim the subject matter which applicant regards as the invention.

All amendments are made in a good faith effort to advance the prosecution on the merits. Applicant reserves the right to subsequently take up prosecution on the claims as

originally filed in this or appropriate continuation, continuation-in-part and/or divisional applications.

Applicant respectfully submits that no amendments have been made to the pending claims for the purpose of overcoming any prior art rejections that would restrict the literal scope of the claims or equivalents thereof.

Applicant respectfully requests that the amendments submitted herein be entered, and further request reconsideration in light of the amendments and remarks contained herein.

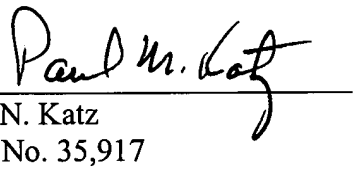
Applicant respectfully requests withdrawal of all objections and rejections, and that there be an early notice of allowance.

SUMMARY

In light of the above amendments and remarks Applicant respectfully submits that the application is now in condition for allowance and early notice of the same is earnestly solicited. Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

Applicant believes that there are no fees due in association with the filing of this Response. However, should the Commissioner deem that any fees are due, including any fees for extensions of time, Applicant respectfully requests that the Commissioner accept this as a Petition Therefor, and direct that any and all fees due are charged to Baker Botts L.L.P. **Deposit Account No. 02-0383**, *(formerly Baker & Botts, L.L.P.)* **Order Number 068354.1446.**

Respectfully submitted,
BAKER BOTTS L.L.P. (023640)

By: 

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